EE150 Digital RTL Design with VHDL

Spring 2017, WF 2:30 - 3:55 ; TBD

- This is a course on **hardware**.

- Detailed study of the VHDL language, with emphasis on the right constructs for optimal physical implementation.

- ASIC-oriented (RTL approach, detailed hardware structures).

- Extensive review of digital design concepts (clock division and multiplication, clock-domains crossing, synchronizers, glitch-free signals, clock gating for power conservation, linear versus log combinational logic, advanced state machines, etc.).

- Circuits are synthesized and tested in state-of-the art FPGAs.

- Preference given to grad students.

Questions: Please email to vpedroni@caltech.edu